REMARKS

In the Office Action dated October 7, 2004, claims 1-25 were presented for examination. The Examiner objected to the Disclosure, and specifically, page 7, line 26. In addition, claims 1-25 were rejected under 35 U.S.C. §102(b).

Applicant wishes to thank the Examiner for the careful and thorough review and action on the merits in this application. The following remarks are provided in support of the pending claims and responsive to the Office Action of October 7, 2004 for the pending application.

I. Objection to the Disclosure

The Disclosure was objected to as containing redundant language at page 7, line 26. The Examiner raised the same objection to this language in the First Office Action dated May 6, 2004 to which Applicant submitted an amendment to this language to remove the redundancy. Accordingly, Applicant respectfully requests the Examiner to enter the correction in the Response to the First Office Action dated August 6, 2004.

II. Rejection of claims 1-25 under 35 U.S.C. §102(b)

Claims 1-25 were rejected under 35 U.S.C. §102(b) as being anticipated by *Hagersten*, U.S. Patent No. 5,749,095. The *Hagersten* patent '095 relates to performing efficient write operations in a multiprocessor computer system. More specifically, *Hendersen* discloses performing write operations prior to completion of a coherency operation if the write operation includes a specific predefined code. The Examiner asserts that cache (18a or 18b) local to each processor may be considered local memory, and that memory (56) is shared memory as it is controlled by a data controller. In fact, memory (56) is local to each sub node, as shown in Fig. 2. Transactions are placed in associated queues for processing. Each subnode includes an address controller (52) that has an out queue (72) and an in queue (74). "Out queue (72) buffers transactions from the processors connected thereto until address controller (52) is granted access

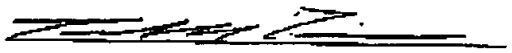
to address bus (58). Address controller (52) performs the transactions stored in out queue (72) in the order those transactions were placed into out queue (72) (i.e. out queue (72) is a FIFO queue)." Col. 11, lines 54-60. "Similar to out queue (72), in queue (74) is a FIFO queue." Col. 11, line 65. Both the in queue (74) and out queue (72) of *Hagersten* '095 places some form of ordering constraints on memory execution by means of the first-in-first-out queue rule implemented in both queues. However, these ordering constraints do not show differentiating between local and non-local memory operations. As shown in Applicant's amended claims 1, 12, and 22, local and non-local memory write operations are handled differently. The local write operations are allowed to execute in an arbitrary order, and a set of non-local write operations are provided a specific order for execution. *Hagersten* does not address differentiating between local and non-local write operation. In fact, *Hagersten* is clear that all operations are conducted in a first-in-first-out (FIFO) basis. The exception to FIFO in *Hagersten* is when an "ignore signal" is employed to affect the ordering of one or more specific transaction. However, neither FIFO or use of the "ignore signal" is equivalent to differentiating between a local and non-local write operations and the constraints placed upon this differentiation by Applicant. Accordingly, the ordering of memory operations of *Hendersen* operate under different parameters and a different environment than that claimed by Applicant.

Applicant's invention applies to write operations to local memory and write operations to non-local memory. There is no teaching in *Henderson* for allowing an arbitrary order of execution of write operations from local memory and placing a specified order of execution on write operations from non-local memory. In order for the claimed invention to be anticipated under 35 U.S.C. §102(b), the prior art must teach all claimed limitations presented by the claimed invention. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F. 2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)). As mentioned above, *Henderson* does not show all of the elements as claimed by Applicant in pending claims 1-25, and specifically amended claims 1, 12, and 22. Specifically, *Hendersen* does not support differentiating between local and non-local memory write operations, and specifically the use of arbitrarily ordering write operations from local

memory in combination with specific ordering of write operations from non-local memory, as shown in Applicant's pending claims. Accordingly, *Hendersen* clearly fails to teach the limitations pertaining to the arbitrary nature of execution of write operations in local memory in combination with explicit ordering of write operations to non-local memory as presented in Applicant's pending claims 1-25.

For the reasons outlined above, withdrawal of the rejection of record and an allowance of this application are respectfully requested.

Respectfully submitted,

By: 

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